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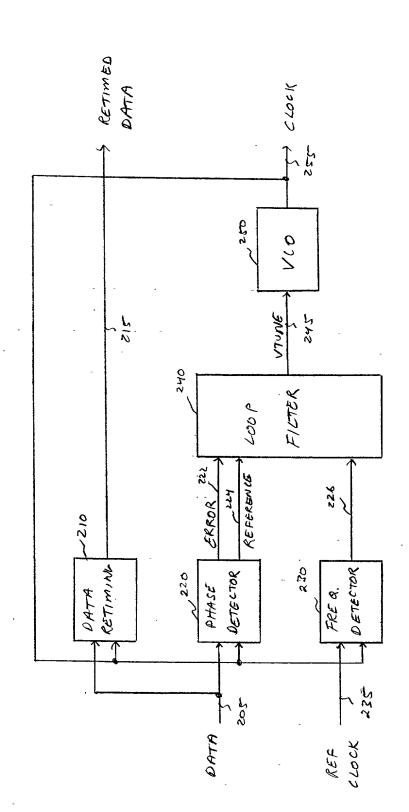


Figure 2

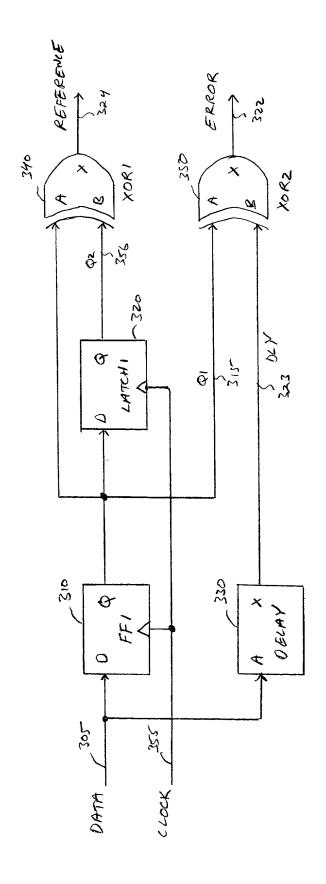
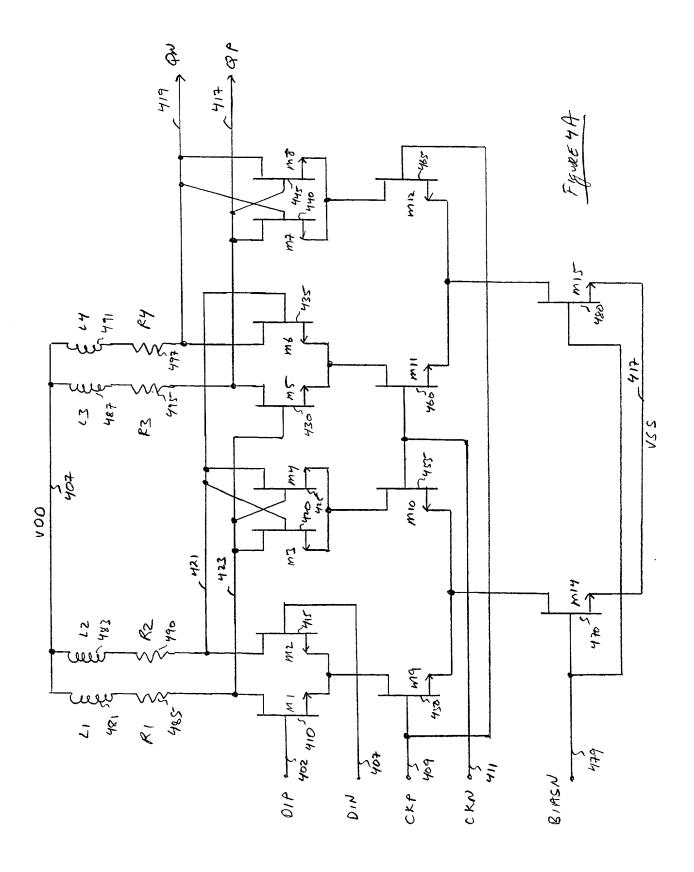
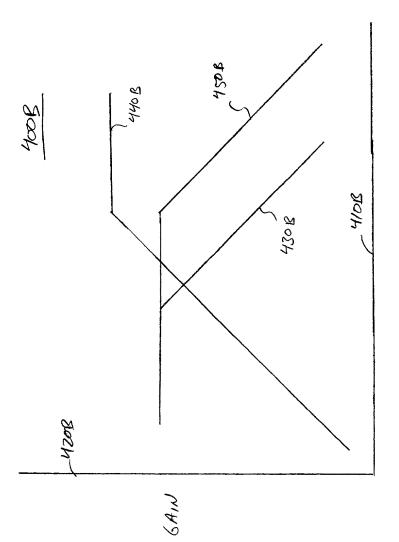


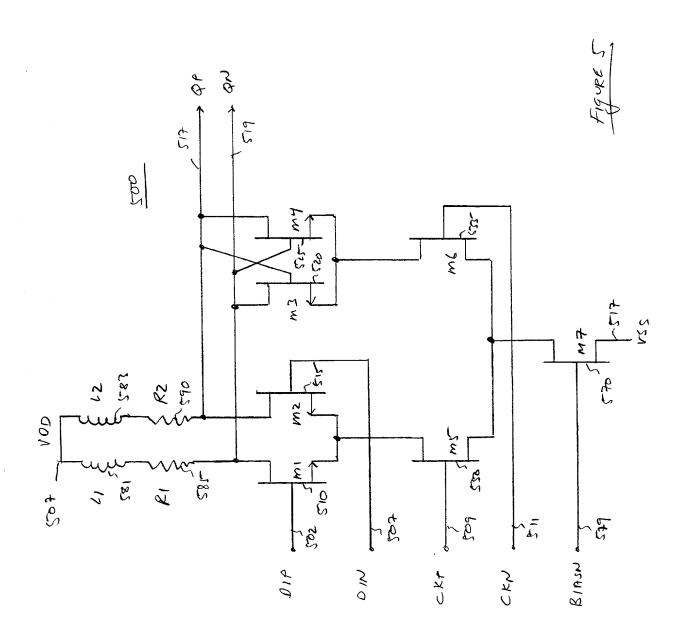
FIGURE 3

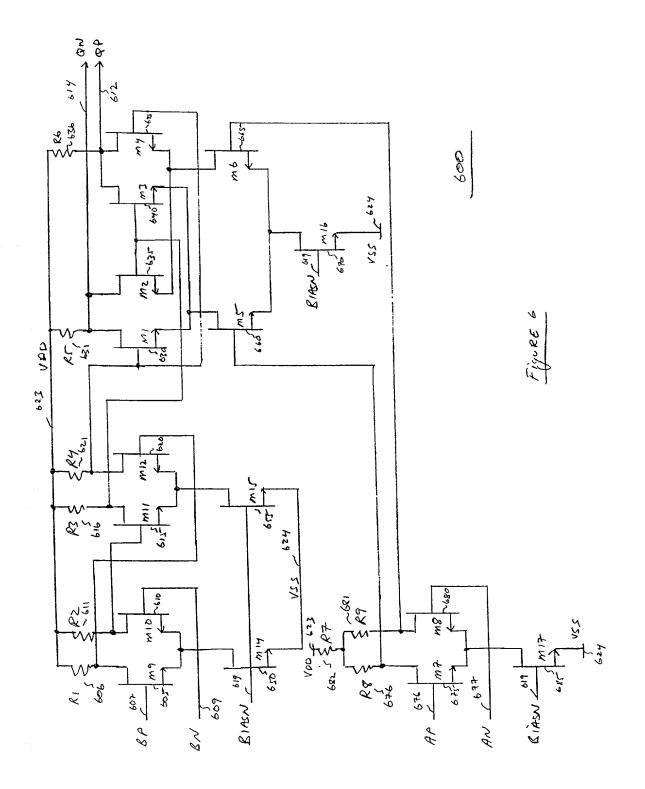


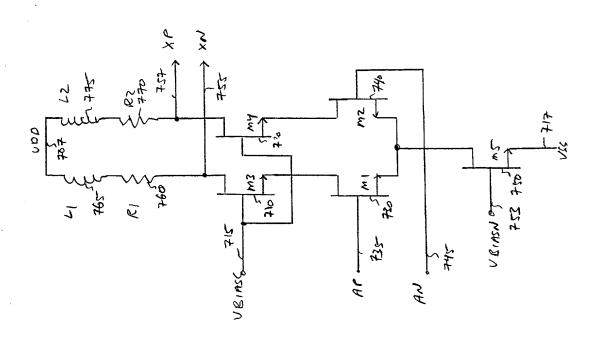


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FLOORE 48



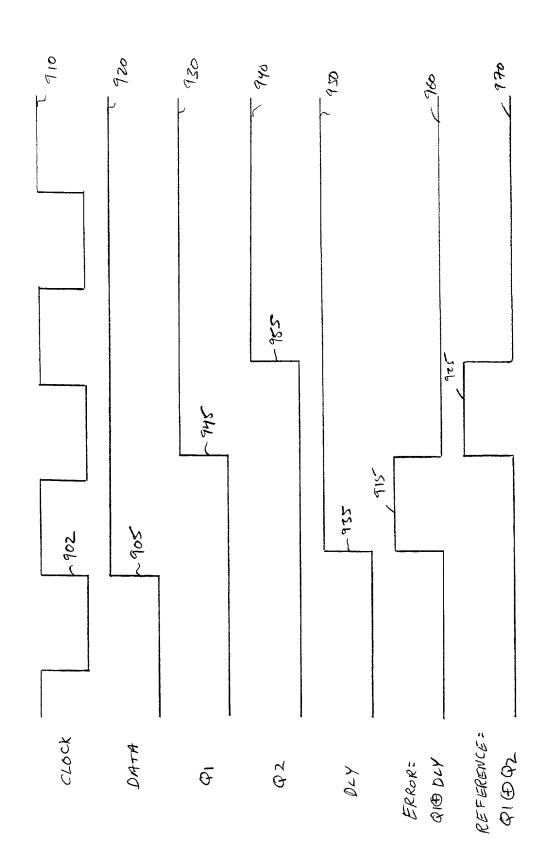




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Figure 8

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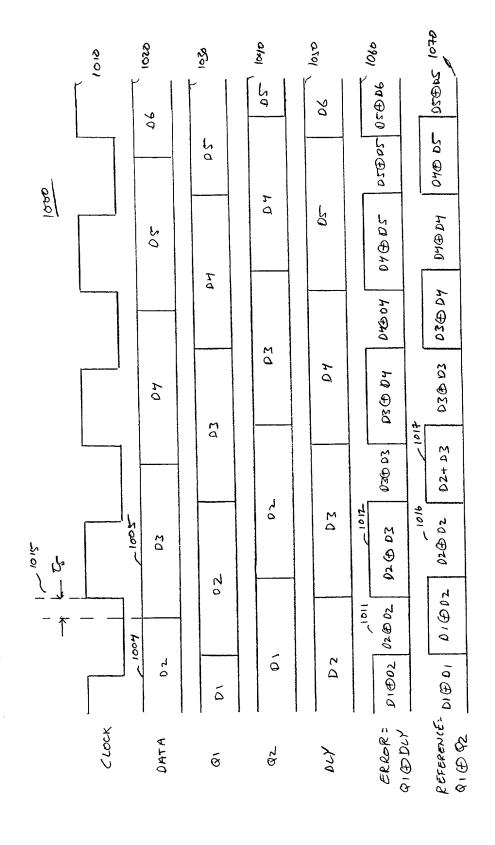


FiguRE 10

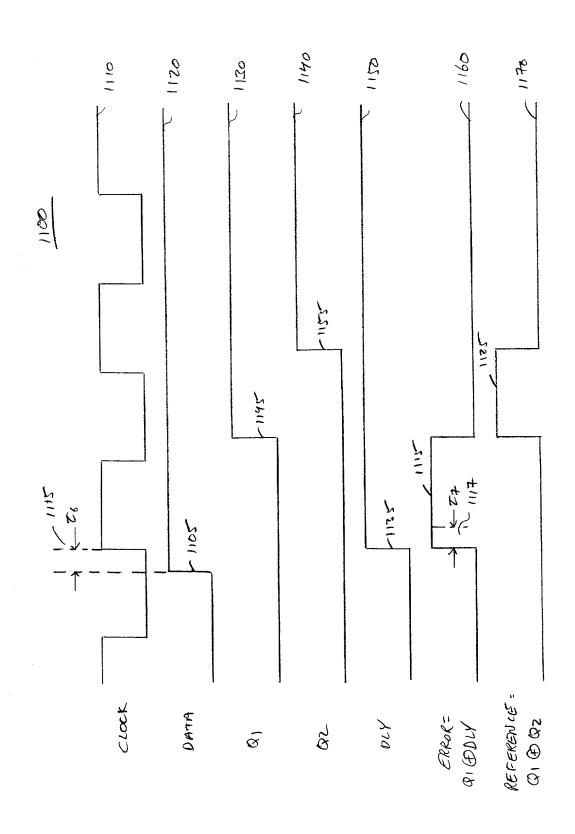


Figure 11

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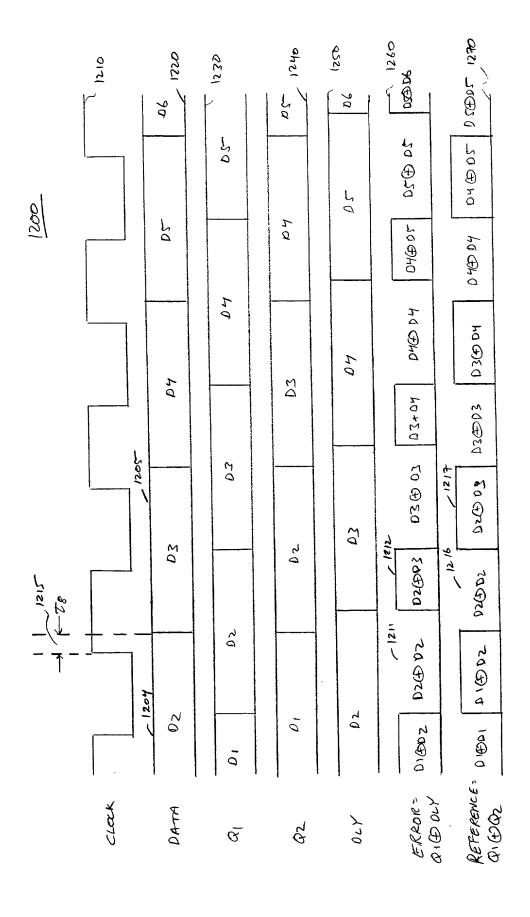
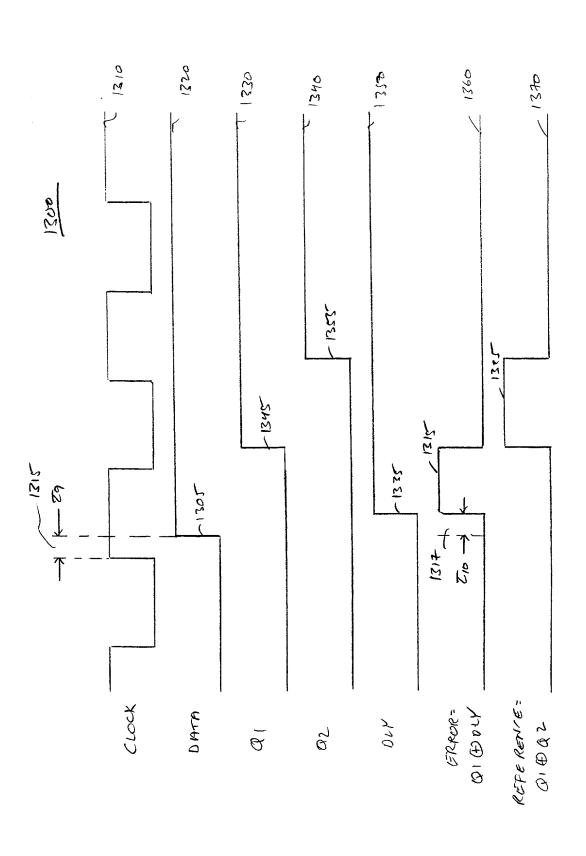
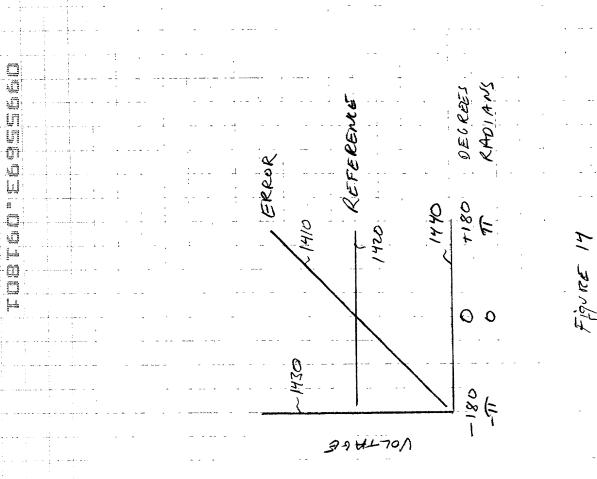


FIGURE 12

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Flore 13



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RECEIVE A DATA INPUT AND A CLOCK INPUT HAVING RISING

AITERNATING BETWEEN HIGH AND LOW

AND FALLING EDGES, AND

FIGURE 15

DELAYED PATA TO GENERATE

AN ERROR SIUNLAL.